ABSTRACT

In a system where multiple instruction pipes share access to a common return stack buffer (RSB), coordination is provided to ensure that no instruction pipe gains unfair access to the RSB. Additionally, further coordination control may be provided to ensure that a pipe operates upon valid data notwithstanding communication delays that may be present in a communication path between the pipe and the RSB. In one embodiment, if a system must gain access to the RSB, it determines with reference to prior accesses to the RSB whether immediate access to the RSB would exceed a predetermined access rate. If so, it delays its attempt to access the RSB until it re-synchronizes to the access rate. In another embodiment, it delays use of data from the RSB until communication delays are overcome.